* Everyone has to add a slide telling about the future prospect of the project which will include (advance verilog circuit, correlation and convolution matrix in image processing and simulation in fpga)
* Intro page - project name, mid-term evaluation, mentors name, group members name,.

**Group-1 (G Sriniketh Balachandar)**

Add image processing slide

Add pictures in python libraries

**Group-2 (Samarth Agarwal)**

Pictures and Left allignment  
Assignment-1 in detail (plots, code pictures)

**Group-3 (Akshit Gupta, vaibhav)**  
Add images in image processing slide

Dont describe a lot(intro of verilog, libraries desc.)

Add images of code, plots

**Group-4 (Manvi Bengani)**

Add Ques done as assignment instead of examples

**Group-5 (Mohd Sarim Ali)**  
Add pictures, plot and images

Add assignment in decoder and half adder

**Group-6 (Shivansh Mangal)**

Add assignment

Add content

**Group-7 (Harsh Verma, Soumya Kumar)**

Remove verilog operator and verilog datyatypes

Image processing - add images of google collab file provided

**Group-8 (Ayush Kumar)**  
Add Fpga and verilog theory

Last slide remove  
Add Little description with pictures